AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of claims in the application.

1-23. (Cancelled).

24. (Currently Amended) A semiconductor integrated device comprising:

a semiconductor substrate;

a plurality of logic circuits formed on said semiconductor substrate and each including a first circuit for inputting a clock signal and a second circuit operating in synchronization with said clock signal input by said first circuit;

an input terminal formed on said semiconductor substrate and receiving an externally supplied power supply voltage;

a first power supply wire ~~to be connected to a predetermined source of electric potential~~ formed on said semiconductor substrate and connected between said input terminal and said first circuit of each of said plurality of said logic circuits; and

a second power supply wire ~~to be connected to the predetermined source of electric potential~~ formed on said semiconductor substrate independently of said first power supply wire and connected between said input terminal and said second circuit of each of said plurality of said logic circuits.

25. (Currently Amended) The semiconductor integrated circuit according to claim 24, wherein

said power supply voltage includes a high-potential side power supply voltage,

said input terminal includes a high-potential side pad electrode ~~receiving said high-potential side pad electrode~~ receiving said high-potential side power supply voltage,

said first power supply wire includes a first high-potential side power supply wire for supplying said high-potential side power supply voltage at said high-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

said second power supply wire includes a second high-potential side power supply wire for supplying said high-potential side power supply voltage at said high-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

26. (Currently Amended) The semiconductor integrated circuit according to claim [[26]] 25, further comprising:

a low-potential side pad electrode formed on said semiconductor substrate and receiving an externally supplied low-potential side power supply voltage; and

a low-potential side power supply wire formed on said semiconductor substrate for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit and said second circuit of each of said plurality of said logic circuits.

27. (Currently Amended) The semiconductor integrated circuit according to claim [[27]] 26, wherein

said low-potential side power supply wire includes

a first low-potential side power supply wire for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

a second low-potential side power supply wire for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

28. (Currently Amended) The semiconductor integrated circuit according to claim [[27]] 26, wherein

said low-potential side pad electrode includes

a first low-potential side pad electrode formed on said semiconductor substrate and receiving said low-potential side power supply voltage and

a second low-potential side pad electrode formed on said semiconductor substrate and receiving said low-potential side power supply voltage,

said low-potential side power supply wire includes

a first low-potential side power supply wire for supplying said low-potential side power supply voltage at said first low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

a second low-potential side power supply wire for supplying said low-potential side power supply voltage at said second low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

29. (Previously Presented) The semiconductor integrated circuit according to claim 24, wherein

said second circuit includes a holding circuit holding the state of an input signal in response to said clock signal input by said first circuit.

30. (Previously Presented) The semiconductor integrated circuit according to claim 24, wherein

said logic circuit is formed by a basic cell of a standard cell system or a gate array system.

31. (Currently Amended) A semiconductor integrated device comprising:

a semiconductor substrate;

a plurality of logic circuits formed on said semiconductor substrate and each including a first circuit for inputting a clock signal and a second circuit operating in synchronization with said clock signal input by said first circuit;

a first input terminal formed on said semiconductor substrate and receiving an externally supplied power supply voltage;

a second input terminal formed on said semiconductor substrate and receiving said externally supplied power supply voltage;

a first power supply wire ~~to be connected to a predetermined source of electric potential~~ formed on said semiconductor substrate and connected between said first input terminal and said first circuit of each of said plurality of said logic circuits; and

a second power supply wire ~~to be connected to the predetermined source of electric potential~~ formed on said semiconductor substrate independently of said first power supply wire and connected between said second input terminal and said second circuit of each of said plurality of said logic circuits.

32. (Currently Amended) The semiconductor integrated circuit according to claim [[37]] 31, wherein

said power supply voltage includes a high-potential side power supply voltage,

said first input terminal includes a first high-potential side pad electrode receiving said high-potential side power supply voltage,

said second input terminal includes a second high-potential side pad electrode receiving said high-potential side power supply voltage,

said first power supply wire includes a first high-potential side power supply wire for supplying said high-potential side power supply voltage at said first high-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

said second power supply wire includes a second high-potential side power supply wire for supplying said high-potential side power supply voltage at said second high-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

33. (Currently Amended) The semiconductor integrated circuit according to claim [[39]] 32, further comprising:

a low-potential side pad electrode formed on said semiconductor substrate and receiving an externally supplied low-potential side power supply voltage; and

a low-potential side power supply wire formed on said semiconductor substrate for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit and said second circuit of each of said plurality of said logic circuits.

34. (Currently Amended) The semiconductor integrated circuit according to claim [[40]] 33, wherein

said low-potential side power supply wire includes

a first low-potential side power supply wire for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

a second low-potential side power supply wire for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

35. (Currently Amended) The semiconductor integrated circuit according to claim [[40]] 33, wherein

said low-potential side pad electrode includes

a first low-potential side pad electrode formed on said semiconductor substrate and receiving said low-potential side power supply voltage and

a second low-potential side pad electrode formed on said semiconductor substrate and receiving said low-potential side power supply voltage,

said low-potential side power supply wire includes

a first low-potential side power supply wire for supplying said low-potential side power supply voltage at said first low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and

a second low-potential side power supply wire for supplyng said low-potential side power supply voltage at said second low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

36. (Currently Amended) The semiconductor integrated circuit according to claim [[37]] 31, wherein

said second circuit includes a holding circuit holding the state of an input signal in response to said clock signal input by said first circuit.

37. (Currently Amended) The semiconductor integrated circuit according to claim [[37]] 31, wherein

said logic circuit is formed by a basic cell of a standard cell system or a gate array system.